

STRUCTURE Silicon Monolithic Integrated Circuit
 TYPE 8ch Analog Multiplexer / Demultiplexer

PRODUCT SERIES **BU4051BC**
BU4051BCF
BU4051BCFV

FEATURES

- Wide operating power supply range(3[V]~18[V])
- High impedance input

○ ABSOLUTE MAXIMUM RATINGS (Ta=25[°C])

Parameter	Symbol	Limit	Unit
Power Supply Voltage1	VDD	(VSS-0.5)~(VSS+20.0)	V
Power Supply Voltage2	VDD-VEE	(VSS-0.5)~(VSS+20.0)	V
Power Dissipation	Pd	BU4051BC	1250(*1)(*4)
		BU4051BCF	380(*2)(*4)
		BU4051BCFV	620(*3)(*4)
Supply current	Iin	± 10	mA
Operating temperature	Topr	-40~+85	°C
Storage temperature	Tstg	-55~+150	°C
Input Voltage	Vin	(VSS-0.5)~(VDD+0.5)	V
Maximum junction temperature	Tjmax	150	°C

- This product is designed for protection against radioactive rays.

(*1) When used at Ta=25[°C] on above, value of above is reduced 10.0[mW] per 1[°C].

(*2) When used at Ta=25[°C] on above, value of above is reduced 3.1[mW] per 1[°C].

(*3) When used at Ta=25[°C] on above, value of above is reduced 5.0[mW] per 1[°C].

(*4) Power dissipation is the value for mounting 70[mm]×[70mm]×1.6[mm] FR4 glass epoxy circuit board (copper foil area is 3% or less).

○ OPERATING CONDITION (Ta=-40~+85[°C])

Parameter	Symbol	Limit	Unit
Power Supply Voltage1	VDD	+3.0~+18.0	V
Power Supply Voltage2	VDD-VEE	+3.0~+18.0	V
Input voltage	VIN	0~VDD	V

Status of this document

The Japanese version of this document is the official specification.

This translated version is intended only as a reference, to aid in understanding the official version.

If there are any differences between the original and translated versions of this document, the official Japanese language version takes priority.

○ ELECTRICAL CHARACTERISTICS (unless otherwise noted, VSS=VEE=0[V], Ta=25[°C])

Parameter	Symbol	Standard Value			Unit	VDD[V]	Condition
		MIN	TYP	MAX			
Input "H" voltage	VIH	3.5	—	—	V	5	—
		7.0	—	—	V	10	
		11.0	—	—	V	15	
Input "L" voltage	VIL	—	—	1.5	V	5	—
		—	—	3.0	V	10	
		—	—	4.0	V	15	
Input "H" current	I _{IH}	—	—	0.3	μA	15	VIH=15[V]
Input "L" current	I _{IL}	—	—	-0.3	μA	15	VIL=0[V]
ON resistance	RON	—	—	950	Ω	5	VIN=VDD/2
		—	—	250	Ω	10	
		—	—	160	Ω	15	
ON resistance defluxion	ΔRON	—	10	—	Ω	5	—
		—	6	—	Ω	10	
		—	4	—	Ω	15	
Channel-OFF Leakage current	IOFF	—	—	0.3	μA	15	—
		—	—	-0.3	μA	15	
Supply current	IDD	—	—	5	μA	5	VIN=GND,VDD
		—	—	10	μA	10	
		—	—	15	μA	15	
Input capacitance	CIN	—	5	—	pF	—	—

○ Switching Characteristics (unless otherwise noted, Ta=25[°C], VSS=VEE=0[V], RL=10[kΩ], CL=50[pF])

Parameter	Symbol	Standard Value			Unit	VDD[V]	Condition
		MIN	TYP	MAX			
Propagation delay time (SW IN → OUT)	t _{PLH} t _{PHL}	—	15	45	ns	5	—
		—	8	20	ns	10	
		—	6	15	ns	15	
Propagation delay time (A,B,C → OUT)	t _{PHZ} t _{PLZ} t _{PZH} t _{PZL}	—	170	550	ns	5	—
		—	90	240	ns	10	
		—	70	160	ns	15	
Propagation delay time (INH → OUT)	t _{PHZ} t _{PLZ} t _{PZH} t _{PZL}	—	150	380	ns	5	—
		—	70	200	ns	10	
		—	50	160	ns	15	
Maximum propagation frequency (*5)	f _{max}	—	20	—	MHz	5	VEE=-5[V]
Feed through attenuation (*6)	F.T	—	0.5	—	MHz	5	VEE=-5[V]
Sine wave distortion (*7)	D	—	0.02	—	%	5	VEE=-5[V]

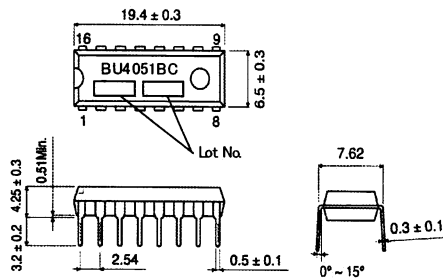
(*5) VIN:5Vp-p Sine wave, frequency where gain is 20log(VOUT/VIN)=-3[dB]

(*6) VIN:5Vp-p Sine wave, frequency where gain is 20log(VOUT/VIN)=-50[dB] at channel Off

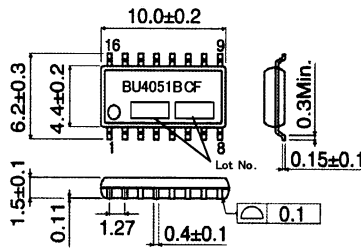
(*7) VIN:5Vp-p Sine wave, f=1[kHz]

*Maximum value is under design guarantee.

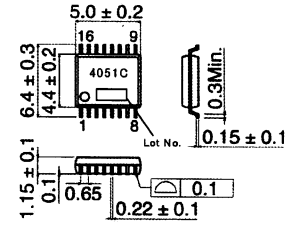
○ PHYSICAL DIMENSIONS



BU4051BC(DIP16)(UNIT:[mm])

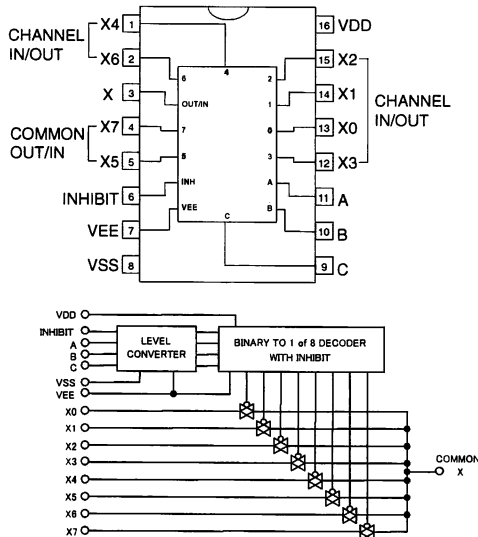


BU4051BCF(SOP16)(UNIT:[mm])



BU4051BCFV(SSOP-B16)(UNIT:[mm])

○ BLOCK DIAGRAM



○ PIN DESCRIPTION

PIN No.	PIN NAME
1	X4
2	X6
3	X
4	X7
5	X5
6	INHIBIT
7	VEE
8	VSS
9	C
10	B
11	A
12	X3
13	X0
14	X1
15	X2
16	VDD

○ NOTES FOR USE

(1) Absolute maximum ratings

Exceeding the absolute maximum ratings, including applied voltage and operating temperature range, may damage or destroy the IC. Since the cause of the damage cannot be conclusively identified (as, for example, a short or open mode), be sure to take appropriate physical safety measures, such as incorporating fuses, whenever a special mode anticipated to exceed absolute maximum ratings is employed.

(2) External voltage at input terminal

$VDD+0.3[V]$, $VSS-0.3[V]$ can be input led without characteristics deterioration and destruction. However the circuit operation is not guaranteed. Please use within recommended operating conditions.

(3) Treatment about input of unused circuit

Redundancy current and oscillation may occur, so untreated input should be connected to VDD or VSS. At connection, it is better to connect resistance (about $100k\Omega$).

(4) Power Dissipation

It the IC is used out of this power dissipation area, the faulty operation or reduction of current characteristics may occur due to the rise of IC temperature. Also, be sure to Use this IC within a power dissipation range while also allowing enough margins.

(5) Mounting errors

Mounting errors, such as incorrect positioning or orientation, may destroy the device.

(6) Electromagnetic fields

Use in strong electromagnetic fields may cause malfunctions. Be careful operating in electromagnetic fields.

(7) Treatment of IC

Stress (camber, bend etc) may cause characteristic change due to piezo electric effect.
Pay attention to stress.

(8) Latch up

Please pay attention to the deterioration and destruction by parasitic element action and latch up that occurs when excessive noise, surge on negatic voltage is loaded at the normal operation.

(9) Test with set PCB

When you connect capacitor to low impedance terminal. You should discharge to avoid stress under IC.
Also at attachment and detachment to jig in testing line, its power supply should be "OFF" .
Moreover for static electricity, please set ground to assembly line, and pong enough attention at conveyance on storage.

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